WHAT IS CLAIMED IS:

1. A memory element comprising a memory cell having an aspect ratio less than one, wherein the aspect ratio is a ratio of a first dimension of the memory cell to a second dimension of the memory cell, the first dimension in the direction of a bit line of the memory element and the second dimension in the direction of a word line of the memory element.

2. The memory element of claim 1, wherein the aspect ratio is less than 0.5.

3. The memory element of claim 1, wherein the memory cell is a 6T memory cell.

4. The memory element of claim 1, wherein the 6T memory cell comprises:

a first inverter having a gating node and a storage node;

a second inverter having a gating node and a storage node, wherein the gating node of the second inverter is coupled to the storage node of the first inverter and the storage node of the second inverter is coupled to the gating node of the first transistor;

a first pass transistor coupled to the storage node of the first inverter; and

a second pass transistor coupled to the storage node of the second inverter.

5. The memory element of claim 4, wherein the first pass transistor includes a control electrode coupled to the word line, a first current conducting electrode coupled to a first bit line of the pair of bit lines, and a second current conducting electrode coupled to the storage node of the first inverter.

6. The memory element of claim 5, wherein the second pass transistor includes a control electrode coupled to the word line, a first current conducting electrode coupled to a second bit line of the pair of bit lines, and a second current conducting electrode coupled to the storage node of the second inverter.

7. The memory element of claim 1, further comprising:

a semiconductor substrate having a major surface; and

a first metallization system disposed over the major surface, wherein the pair of bit lines comprise a portion of the first metallization system.

8. The memory element of claim 7, further including a second metallization system over the first metallization system, wherein the word line comprises a portion of the second metallization system.

9. The memory element of claim 8, further including a first shielding element adjacent one side of the word line.

10. The memory element of claim 9 further including a second shielding element adjacent an opposing side if the word line.

11. A memory element, comprising:

a substrate having a major surface;

a memory cell formed from the substrate, the memory cell including at least one silicided portion;

a first layer of dielectric material disposed over the major surface and the at least one silicided portion;

a bit line metallization system disposed over the first layer of dielectric material; and

a word line metallization system disposed over the bit line metallization system.

12. The memory element of claim 11, wherein the memory cell comprises a 6T memory cell.

13. The memory element of claim 12, wherein the 6T memory cell comprises:

a first doped region of a first conductivity type, the first doped region having a first pass transistor area and a first driver area;

a second doped region of a second conductivity type, the second doped region abutting the first doped region;

a first gate structure having first and second sides disposed over the first transistor area, wherein a first portion of the first pass transistor area adjacent the first side of the first gate structure is coupled to a first bit line; and

a second gate structure having first and second sides disposed over the first driver area and over the second doped region, wherein a portion of the first driver area adjacent the first side of the second gate structure is between the first side of the second gate structure and the second side of the first gate structure and wherein a portion of the first driver area adjacent the second side of the second gate structure is coupled for receiving a first source of operating potential.

14. The memory element of claim 13, wherein the first and second gate structures are substantially parallel to each other.

15. The memory element of claim 13, further including:

a third doped region, the third doped region of the first conductivity type and having a second pass transistor area and a second driver area;

a fourth doped region of the second conductivity type, the fourth doped region abutting the third doped region;

a third gate structure having first and second sides disposed over the second pass transistor area, wherein a first portion of the second pass transistor area adjacent the first side of the third gate structure is coupled to a second bit line; and

a fourth gate structure having first and second sides disposed over the second driver area and over the fourth doped region, wherein a portion of the second driver area adjacent the first side of the fourth gate structure is between the first side of the fourth gate structure and the second side of the third gate structure and wherein a portion of the second driver area adjacent the second side of the fourth gate structure is coupled for receiving the first source of operating potential.

16. The memory element of claim 15, wherein the first, second, third, and fourth gate structures are substantially parallel to each other.

17. The memory element of claim 15, wherein a width of the first driver area is greater than a width of the first pass transistor area and a width of the second driver area is greater than a width of the second pass transistor area.

18. The memory element of claim 15, wherein the first doped region cooperates with the second doped region to form a first rectangular shaped region having first and second opposing sides, and wherein a first U-shaped gap extends into the first rectangular shaped region from the first side and a first rectangular extension extends from the second side, and wherein the third doped region cooperates with the fourth doped region to form a second rectangular shaped region having first and second opposing sides, and wherein a second U-shaped gap extends into the second rectangular shaped region from the first side and a second rectangular extension extends from the second side.

19. The memory element of claim 15, wherein the first rectangular shaped region is adjacent to the second rectangular shaped region and wherein the first and second U-shaped gaps face opposite directions from each other, the first and second rectangular extensions extend in opposite directions from each other, and the first U-shaped region faces the same direction that the second rectangular extension extends.

20. The memory device of claim 11, wherein the substrate is a silicon-on-insulator substrate.

21. A method for manufacturing a memory device, comprising:

providing a substrate;

forming first, second, third, and fourth doped regions in the substrate, the first and third doped regions of a first conductivity type and the second and fourth doped regions of a second conductivity type, wherein the first and second doped regions abut each other and the third and fourth doped regions abut each other and are spaced apart from the first and second doped regions;

forming a first gate structure over a portion of the first doped region;

forming a second gate structure over another portion of the first doped region and over the second doped region;

implanting dopant of the second conductivity type into the portions of the first doped region adjacent the first and second gate structures;

implanting dopant of the first conductivity type into the portions of the second doped region adjacent the second gate structure;

forming a bit line metallization system over the substrate, the bit line metallization system electrically coupled to the portion of the first doped region adjacent a first side of the first gate structure; and

forming a word line metallization system over the bit line metallization system, the word line metallization system electrically coupled to the first gate structure.

22. The method of claim 21, further including:

forming a third gate structure over a portion of the third doped region;

forming a fourth gate structure over another portion of the third doped region and over the second doped region;

implanting dopant of the second conductivity type into the portions of the third doped region adjacent the third and fourth gate structures; and

implanting dopant of the first conductivity type into the portions of the fourth doped region adjacent the fourth gate structure.

23. The method of claim 22, wherein forming the first and second doped regions includes:

forming a first masking layer over the substrate, the masking layer having an opening exposing a first portion of the substrate; and

doping the first portion of the substrate with a dopant of the first conductivity type.

24. The method of claim 23, wherein forming the second doped region includes:

forming a second masking layer over the substrate, the second masking layer having an opening exposing a second portion of the substrate, the second portion being a sub-portion of the first portion of the substrate; and

doping the second portion of the substrate with a dopant of the second conductivity type.

25. The method of claim 24, wherein forming the first, second, third, and fourth gate structures comprises:

forming a layer of dielectric material over the substrate;

forming a layer of polysilicon over the layer of dielectric material; and

patterning the layer of polysilicon and the layer of dielectric material.

26. The method of claim 25, wherein forming the bit line metallization system includes:

forming a layer of dielectric material over the substrate;

forming a plurality of trenches in the layer of dielectric material; and

forming an electrically conductive material in the plurality of trenches.